Course Quiz – Digital Logic Design: Combinational Logic

1. The twos' complement of the decimal number 84 (0x54 in hexadecimal) is
    a. 10100011
    b. 10110101
    c. 10101100
    d. 11001011

2. Using Boolean algebra, simplify the expression (A' + B)'.
    a. AB'
    b. A + B'
    c. A'B
    d. A' + B

3. Convert the binary number 1110001011000111
    a. 0xBC35
    b. 0x8613
    c. 0xD2C3
    d. 0xE2C7

4. Using Boolean algebra, simplify the expression AB + ABC.
    a. C
    b. AB
    c. ABC
    d. BC

5. Using Boolean algebra, simplify the expression (A' + B')(A + B').
    a. B'
    b. A'
    c. A'B' + AB'
    d. A + B

6. The binary approximation of the decimal number 137.57 is
    a. 10001001.010111001
    b. 10101100.101010010
    c. 10101100.011011011
    d. 10001001.100100011

7. The fundamental logic gates are _____.
    a. NAND, NOR
    b. AND, OR, NOT
    c. XOR, NAND, NOR
    d. OR, NOR, XOR, XNOR

8. An XOR function yields the expression _____.

    a. AB
    b. A + B
    c. A'B + AB'
    d. (AB)'

9. Convert the product-of-sums (A + B)(A' + C) to a sum-of-products by distributing the terms.

    a. AC + BC
    b. AC + A'B + BC
    c. AA' + A'B + BC
    d. BB' + C

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

10. The truth table above describes the expression _____.

    a. A'B'C' + A'BC' + ABC
    b. A'BC + AB'C
    c. A'BC' + ABC'
    d. A'B'C + A'BC' + ABC'

11. In order to simplify an expression that contains 4 variables, a Karnaugh map can be used that has a _____ grid.

    a. 2 x 2
    b. 2 x 4
    c. 4 x 8
    d. 4 x 4

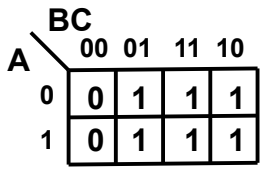
A \ BC	00	01	11	10
0	1	1	0	0
1	1	1	1	0

12. The Karnaugh map shown above is associated with the (non-optimal) expression _____.

a. F = A’B’C’ + A’BC’ + AB’C + ABC’
b. F = A’B’C’ + A’B’C + AB’C’ + AB’C + ABC
c. F = A’B’C + AB’C’ + AB’C
d. F = A’BC’ + A’BC + ABC’

13. The Karnaugh map in the previous problem yields the optimal expression _____.

a. F = A’ + BC
b. F = A’B + BC’
c. F = B’ + AC
d. F = AC’



14. The Karnaugh map shown above yields the optimal expression _____.

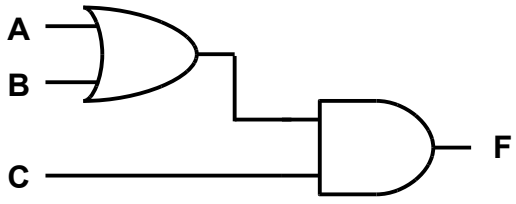
a. F = B’C + BC + BC’
b. F = B + C
c. F = A + B + C
d. F = AB + BC

15. Convert the hexadecimal number 0xAB83 to binary

a. 1011100100010011
b. 1010101110000011
c. 1110001110101001
d. 1011000101101010

16. _____ gates have functional completeness. This means that any logic function can be realized using only this gate.

a. AND
b. OR
c. NAND
d. XOR



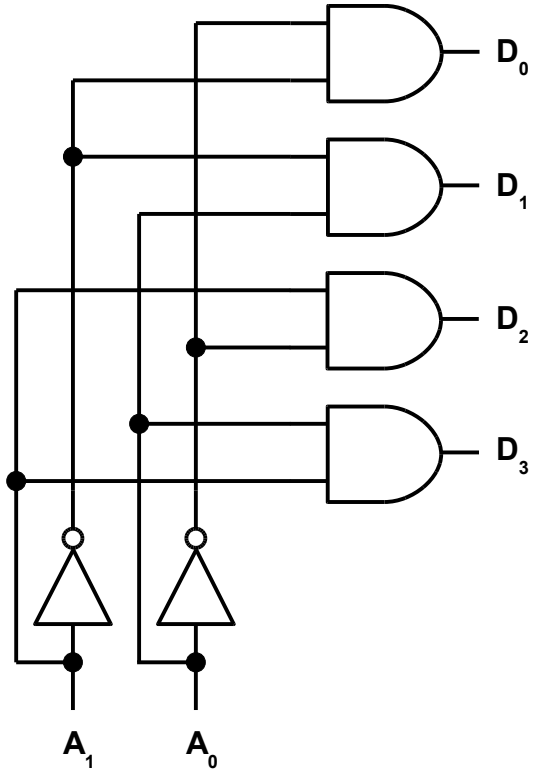
17. The combinational logic diagram shown above produces the expression _____.

a. AB + C

b. A + B + C
c. ABC
d. F = (A + B)C

18. A demultiplexer is different from a decoder because _____.

a. only a decoder has select lines
b. a demultiplexer has a data input while a decoder does not
c. a demultiplexer does not have any output
d. there is no difference



19. For a 2-to-4 decoder shown above, an output of $D_3D_2D_1D_0$ of 0100 would result with an input of A_1A_0 of _____.

a. 11
b. 00
c. 10
d. 01

20. For the 2-to-4 decoder shown above, an output of _____ would result with an input of A_1A_0 equal to 00.

a. $D_0 = 1$
b. $D_1 = 1$
c. $D_2 = 1$
d. $D_3 = 1$

21. A 4-to-1 multiplexer has _____ inputs using 2 data select lines.

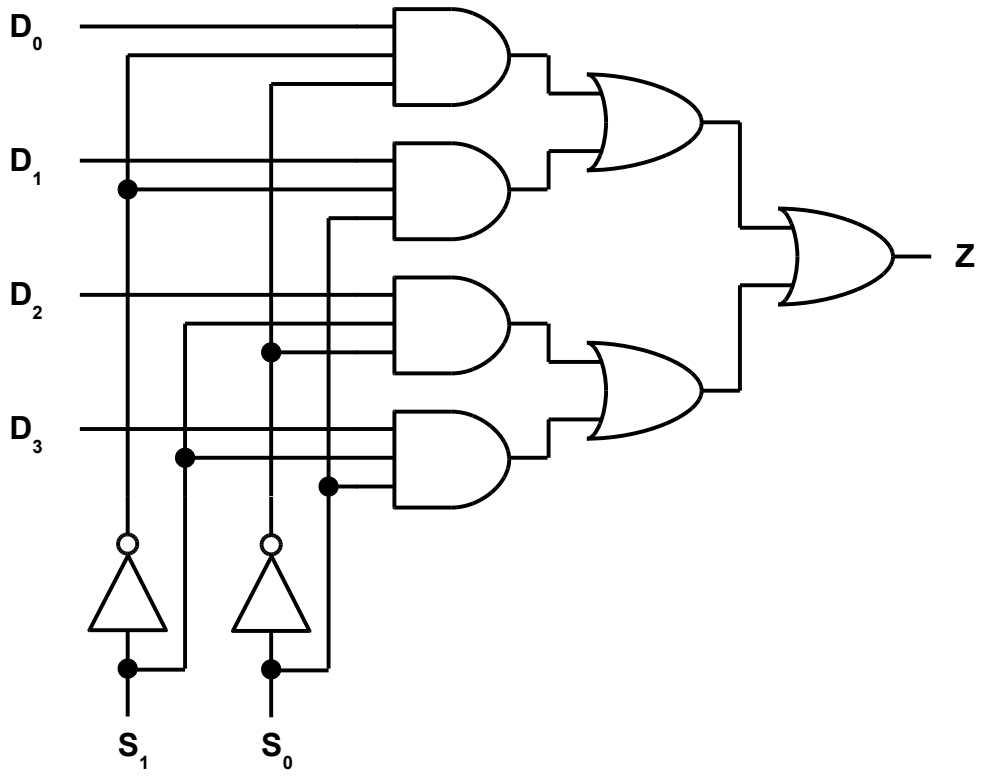
    a. 4
    b. 1
    c. 2
    d. 8

22. A _____ is used in digital systems to select a particular data path to be processed or stored. They allow several signals to share one resource like a data bus.

    a. demultiplexer
    b. decoder
    c. adder
    d. multiplexer

23. A _____ takes a single input and routes it to one of many outputs. It is the opposite of a multiplexer.

    a. decoder
    b. encoder
    c. demultiplexer
    d. full adder



24. For the 4-to-1 multiplexer shown above, what input on the data select lines S_1S_0 will route the input D_2 to the output Z?

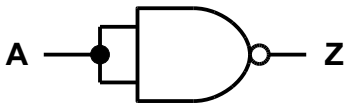
a. 01
b. 11
c. 10
d. 00

25. For the 4-to-1 multiplexer shown above, an input of 11 will route which input to the output Z.

a. D_2
b. D_3
c. D_0
d. D_1

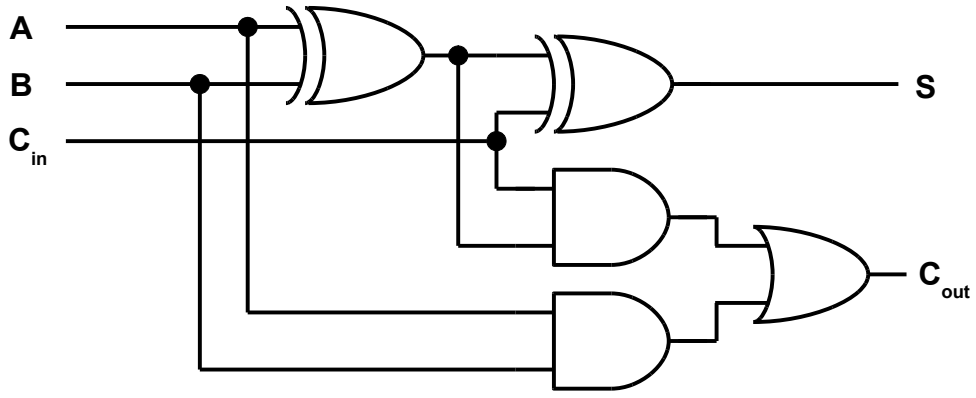
26. An adder that has two inputs A and B has two outputs, S (sum) and _____?

a. subtract
b. add
c. remainder
d. carry



27. The logic diagram shown above implements which basic logic function?

a. AND
b. NOT
c. OR
d. XOR



28. The logic diagram shown above is for a full adder. For an input of A = 1, B = 1, C_{in} = 0, the output will be _____.

a. $C_{out} = 0$, S = 1
b. $C_{out} = 0$, S = 0
c. $C_{out} = 1$, S = 0

d. $C_{out} = 1, S = 1$

29. For the full adder shown above, an input of A = 0, B = 0, $C_{in} = 1$ will produce an output of _____.

    a. $C_{out} = 1, S = 0$
    b. $C_{out} = 0, S = 0$
    c. $C_{out} = 1, S = 1$
    d. $C_{out} = 0, S = 1$

30. Adders can be connected together in a cascaded format starting with a half adder for the least significant bit then followed by multiple full adders ending with the most significant bit. This will allow binary numbers larger than one bit to be added together. This device is called a _____.

    a. ripple carry adder
    b. half adder
    c. full adder
    d. decoder