Final Exam – The Basics of Microcontrollers

1. The difference between a microcontroller and a microprocessor is that _____.
    a. microcontrollers are specialized microprocessors
    b. microcontrollers sometimes contain internal data and program memory whereas microprocessors usually do not contain any internal memory
    c. microcontrollers usually contain peripherals such as communication controllers
    d. all of the above

2. This is a list of all possible instructions that can be interpreted by the CPU. It can be thought of as the processor's vocabulary.
    a. compiler
    b. dictionary
    c. register bank
    d. instruction set

3. A file containing a series of ones and zeros that is interpreted by the central processing unit that instructs the processor to carry out a series of instructions is called _____.
    a. the C programming language
    b. a compiler
    c. machine code
    d. an assembler

4. A series of sequential instructions executed by the CPU is called a _____. It is what software engineers write in a higher level language like C/C++.
    a. memory
    b. multiplexer
    c. program
    d. decoder

5. All of the following are processor architectures except the _____.
    a. Harvard architecture
    b. von Neumann architecture
    c. Babbage architecture
    d. modified Harvard architecture

6. The differences in the processor architectures discussed in the course focus on _____.
    a. processor speed
    b. program memory and data memory access
    c. the number of transistors
    d. the number of registers in the core

7. The advantage of a processor designed with a von Neumann architecture is that simultaneous access to program and data are possible.
    a. true
    b. false

8. The main components of the CPU are the following except _____.
    a. the ALU
    b. flash memory
    c. the control unit
    d. registers

9. The ALU performs _____.
    a. addition, subtraction, multiplication, division
    b. AND, OR, NOT, XOR, bit shifting
    c. logical comparisons
    d. all of the above

10. A processor incorporating a Harvard architecture contains an address 0x00000000 for program memory and an address 0x00000000 for data memory.
    a. true
    b. false

11. Which of the following characteristics best describes a modified Harvard architecture?
    a. data memory starts at address 0x00000000 and program memory starts at address 0x00000000
    b. program and data memories share the same bus to the CPU
    c. the processor has a single address space
    d. program memory and data memory must be stored on the same memory device

12. All of the following characteristics describe a processor with a von Neumann architecture except _____.
    a. the program instructions and data are located in the same memory space
    b. code and data can exist in the same memory space
    c. one bus is used for both program and data memory
    d. one bus is used for program memory and a separate bus is used for data memory

13. The two's complement of 58 is _____.
    a. 1001 1100
    b. 1100 1000
    c. 0101 1100
    d. 1010 1000

14. To multiply a number by 4 you would _____.
    a. shift the number left by one bit
    b. shift the number right by two bits
    c. shift the number left by two bits
    d. shift the number left by four bits

15. What best describes the function of the control unit?
    a. it performs addition and subtraction
    b. it performs logical comparisons
    c. it performs two's complement on a register
    d. it configures the ALU, memory and register bank for a particular operation

16. Half duplex communications means that _____.
    a. every device has a unique address
    b. the device cannot transmit and receive simultaneously
    c. the slaves need a chip select
    d. the device can transmit and receive simultaneously

17. The _____ communications peripheral is half duplex.
    a. UART
    b. timer
    c. SPI
    d. I^2C

18. Synchronous communications means that _____.
    a. the slaves need a chip select
    b. a clock is sent with the data on a separate line
    c. there is a data line but no clock line
    d. the communications link is slow

19. The _____ communications peripheral is asynchronous.
    a. UART
    b. SPI
    c. port
    d. I^2C

20. A device that measures elapsed time or controls events during a predetermined interval is called a _____.
    a. register
    b. timer
    c. flip-flop
    d. GPIO

21. A timer overflow occurs after _____.
    a. the timer is initialized
    b. the ALU completes a move operation

c. the CPU starts to overheat
d. the timer's counter register fills up

22. The name for a temporary storage area for an instruction or piece of data is a _____.
    a. UART
    b. timer
    c. register
    d. byte

23. The _____ cycle governs the CPU's operation.
    a. fetch-decode-execute
    b. fetch-deliver-execute
    c. fetch-deliver-program
    d. program-decode-execute

24. The _____ CPU cycle configures the ALU for a particular operation.
    a. run
    b. decode
    c. memory
    d. deliver

25. The _____ component decodes an instruction from the program code.
    a. clock
    b. control unit
    c. ALU
    d. register

26. General purpose input/output is best described as _____.
    a. a single pin that can be set high or low as an output or can be read as an input
    b. a UART
    c. an address bus
    d. a data bus

27. The _____ has an input frequency of 32768 Hz, does not go to sleep with the processor and may or may not contain an integrated calendar.
    a. universal asynchronous receiver/transmitter
    b. core
    c. arithmetic logic unit
    d. real-time clock

28. The _____ communications peripheral requires a chip select.
    a. UART
    b. interrupt
    c. SPI
    d. I^2C

29. The _____ communications peripheral requires the sender (or master) to send the address of the receiver (or slave).
    a. UART
    b. SPI
    c. port
    d. I^2C

30. The _____ communications peripheral usually is used in conjunction with a transceiver (such as RS-232 or RS-485) to communicate with a device on another circuit board.
    a. UART
    b. SPI
    c. Ethernet
    d. I^2C