FluxLight
OPTICAL TRANSCEIVERS

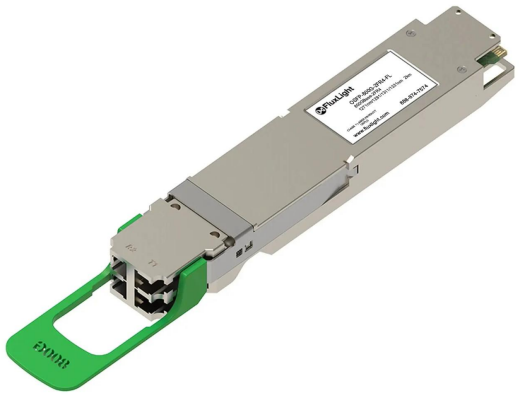
Datasheet

OSFP-800G-2FR4-A-FL

800G, OSFP, Dual Duplex LC, 2x400G-FR4, SMF, 2km, COM

Quick Spec

Rate Category:	800G
Form Factor:	OSFP (twin-port, closed finned top)
Interface Type:	2x400G-FR4
Standard / Protocol:	IEEE 802.3cu 400GBASE-FR4 and 100G Lambda MSA 400G-FR4 ×2; IEEE 802.3ck 800GAUI-8 electrical; CMIS
TX Wavelength:	1271/1291/1311/1331nm (CWDM)
RX Wavelength:	1271/1291/1311/1331nm (CWDM)
Cable Type:	SMF
Reach:	2km (SMF) with host FEC
DDM:	Supported (CMIS)
Connector Type:	Dual Duplex LC (UPC)
Power Consumption:	15W max
Operating Temperature:	0°C to +70°C



Overview

The FluxLight OSFP-800G-2FR4-A-FL is an 800Gb/s twin-port OSFP transceiver for single-mode links up to 2 km. It carries two independent 400G-FR4 links in one module. On the transmit side, each half takes four 106.25Gb/s PAM4 electrical lanes (800GAUI-8, IEEE 802.3ck). It converts them to four optical signals on the CWDM grid at 1271, 1291, 1311 and 1331 nm (ITU-T G.694.2) and multiplexes them onto a single fiber. The receive side demultiplexes the four wavelengths and converts them back to four electrical lanes. The optical interface is two duplex LC (UPC) receptacles, based on IEEE 802.3cu 400GBASE-FR4 and the 100G Lambda MSA 400G-FR4, and full 2 km reach requires KP4 FEC on the host.

The module uses a silicon photonics design with two sets of four-lane CWDM MUX/DEMUX. It is managed via CMIS over the two-wire serial (I2C) interface and provides per-lane digital diagnostics. Selectable application modes let it run as 2×400G FR4, 2×200G FR4 or 2×100G CWDM4 on Ethernet hosts, and as InfiniBand NDR, HDR or EDR links on InfiniBand hosts. It draws 15 W maximum from a single +3.3V supply, and the closed-top finned housing is made for air-cooled OSFP switch ports. Every FluxLight optic is programmed and tested for 100% compatibility with the target OEM platform and is backed by a lifetime warranty.

Features

- 800Gb/s twin-port OSFP, hot-pluggable
- Two independent 400G-FR4 links per module (2×400G)
- Electrical interface: 8 × 106.25Gb/s PAM4, 800GAUI-8 per IEEE 802.3ck
- Optical interface: 2 × 4 CWDM lanes at 53.125 GBd PAM4, based on IEEE 802.3cu 400GBASE-FR4 and 100G Lambda MSA 400G-FR4
- CWDM wavelengths: 1271 / 1291 / 1311 / 1331 nm (ITU-T G.694.2)
- Silicon photonics design with two sets of four-lane CWDM MUX/DEMUX
- Up to 2 km over single-mode fiber with host-side KP4 FEC
- Dual duplex LC (UPC) connectors
- Average launch power −3.2 to +3.5 dBm per lane; stressed receiver sensitivity −2.6 dBm (OMAouter) per lane
- Supports 2×400G FR4, 2×200G FR4 and 2×100G CWDM4 application modes
- CMIS management with per-lane DDM (Tx power, Tx bias, Rx power), case temperature and supply voltage monitoring
- Tx and Rx LOS/LOL and Tx fault indication
- Host- and line-side loopback and PRBS generator/checker
- CDB firmware upgrade
- Closed-top finned housing for air-cooled OSFP ports
- Single +3.3V supply, 15W max power consumption
- Operating case temperature: 0°C to +70°C (COM)
- Class 1 laser product (IEC/EN 60825-1)
- RoHS compliant
- 100% compatible with and programmed for the target OEM platform
- Backed by a FluxLight lifetime warranty

Applications

- 800G (2×400G) Ethernet over single-mode fiber up to 2 km
- InfiniBand NDR, HDR and EDR links
- Spine/leaf and switch-to-switch links within and between data center buildings
- Telecom networks
- Splitting one 800G OSFP port into two 400G-FR4 links
- Backward-compatible links to 200G FR4 and 100G CWDM4 equipment

CMIS Application Advertisements

ApSel Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 1	50 (400GAUI-4-L C2M)	1D (400GBASE-FR4)	44 (4:4)	11 (lanes 1,5)
ApSel 2	32 (IB NDR53G)	1D (400GBASE-FR4)	44 (4:4)	11 (lanes 1,5)
ApSel 3	0F (200GAUI-4 C2M)	18 (200GBASE-FR4)	44 (4:4)	11 (lanes 1,5)

CMIS Application Advertisements (Continued)

ApSel Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 4	31 (IB HDR26G)	18 (200GBASE-FR4)	44 (4:4)	11 (lanes 1,5)
ApSel 7	4F (400GAUI-4-S C2M)	1D (400GBASE-FR4)	44 (4:4)	11 (lanes 1,5)
ApSel 10	42 (CAUI-4 C2M with RS FEC)	10 (100G CWDM4 MSA)	44 (4:4)	11 (lanes 1,5)
ApSel 11	30 (IB EDR25G)	10 (100G CWDM4 MSA)	44 (4:4)	11 (lanes 1,5)

Table 1. CMIS Application Advertisements

Pin Map and Description

The electrical interface of the OSFP module consists of a 60-contact edge connector, as illustrated in Figure 1 and defined in Clause 8.1 of the OSFP MSA Specification.

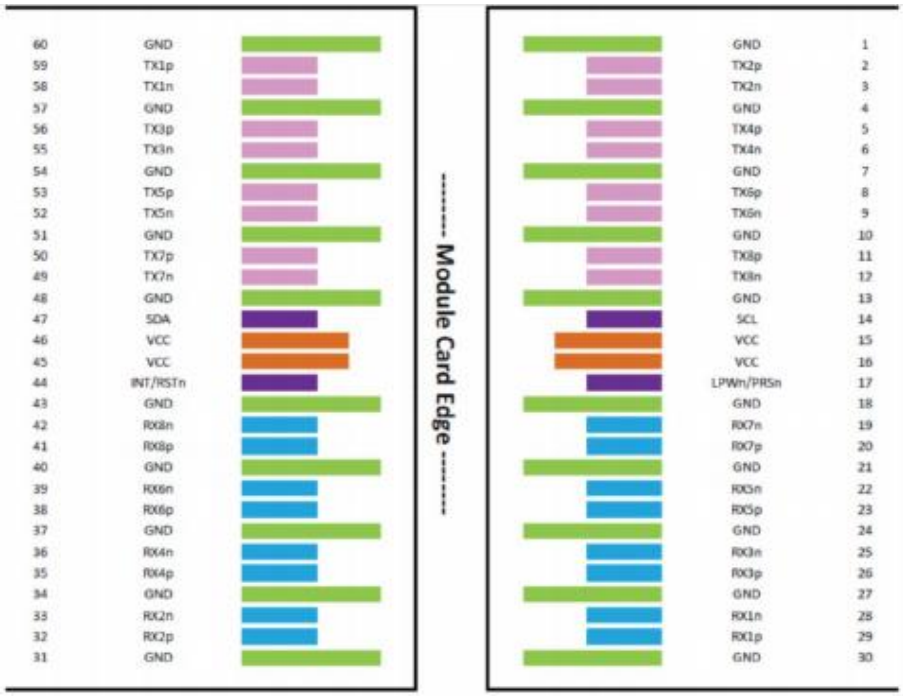


Figure 1. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3

Pin Map and Description (Continued)

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3

Pin Map and Description (Continued)

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Table 2. OSFP Connector Pin List

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

Pin Map and Description (Continued)

Name	Direction	Description
LPWn/ PRSn	Input/Output	Dual Function Signal. - Low Power mode is an active-low input signal. - Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal - Voltage zones are shown in Figure 2.
INT/RSTn	Input/Output	Dual Function Signal. - Reset is an active-low input signal. - Interrupt is an active-high output signal - Voltage zones are shown in Figure 2.

Table 3. OSFP Control Pins

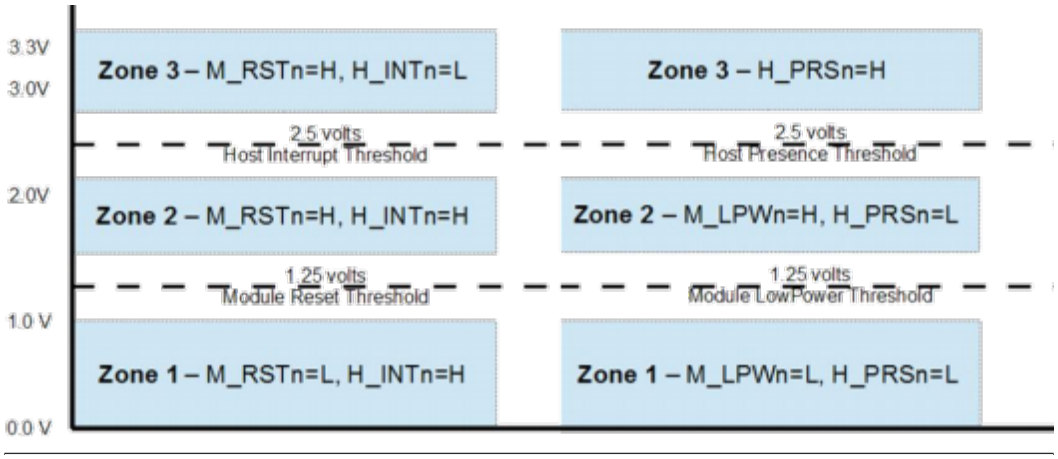


Figure 2. Voltage Zones

Recommended Power Supply Filter

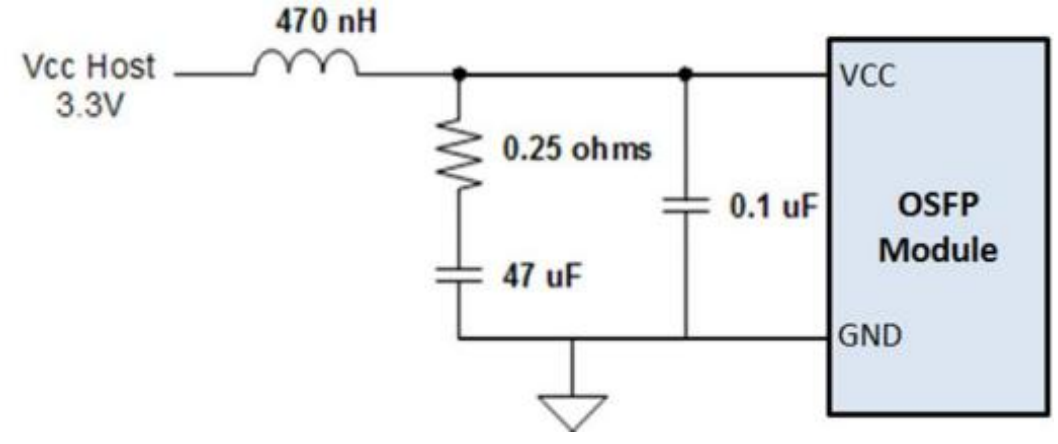


Figure 3. Recommended Power Supply Filter

Optical Port Description

The optical interface port is dual duplex LC. The transmit and receive optical lanes shall occupy the positions depicted in Figure 4 when looking into the MDI receptacle with the connector keyway feature on top.

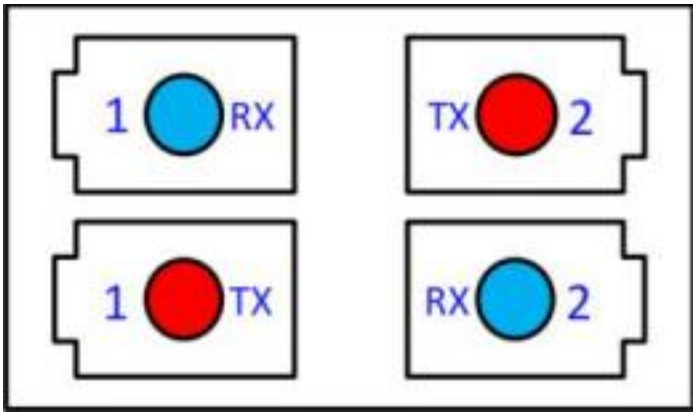


Figure 4. Optical Media Dependent Interface port assignments

Absolute Maximum Ratings

Operation in excess of any individual absolute maximum rating may cause permanent damage to the module.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Power Supply Voltage	V_{CC}	-0.3	3.6	V
Relative Humidity (non-condensation)	RH	5	85	%
Damage Power	P_{max}	5.7		dBm
ESD, electrical pins	ESD	-1	1	kV

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-15}		1
Link Distance	D	0.002		2	km	2

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units
Power Consumption				15	W
Supply Current	Icc			4.5	A
Module Input (each Lane)					
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd
DC Common-mode input Voltage	TP1	-0.35		2.85	V
Single-ended input Voltage	TP1a	-0.4		3.3	V
AC Common-mode RMS input Voltage Low-frequency, VCM_{LF} Full-Band, VCM_{FB}	TP1a	 32 80			mV
Module stressed input test		IEEE 802.3ck 120G3.4.3			
Differential Peak-to-Peak input Voltage tolerance	TP1a	750			mV
Common-mode to Differential-mode Input Return Loss	TP1	IEEE802.3ck Equation 120G-2			
Effective input Return Loss	TP1	8.5			dB
Differential input Termination Mismatch	TP1			10	%
Module Output (each Lane)					
Signaling Rate, each lane	TP4	53.125 ± 100 ppm			GBd
Differential Peak-to-Peak Output Voltage Short mode Long mode	TP4			 600 845	mV
AC Common Mode Output Voltage, RMS Low-frequency, VCM_{LF} Full-Band, VCM_{FB}	TP4			 32 80	mV
Differential Termination Mismatch	TP4			10	%
Eye height	TP4	15			mV
Vertical eye closure, VEC	TP4			12	dB
Common-mode to Differential-mode Output Return Loss	TP4	IEEE802.3ck Equation 120G-1			dB
Effective output Return Loss	TP4	8.5			dB
Output Transition time (20% to 80%)	TP4	8.5			ps
DC Common-mode output Voltage	TP4	-350		2850	mV

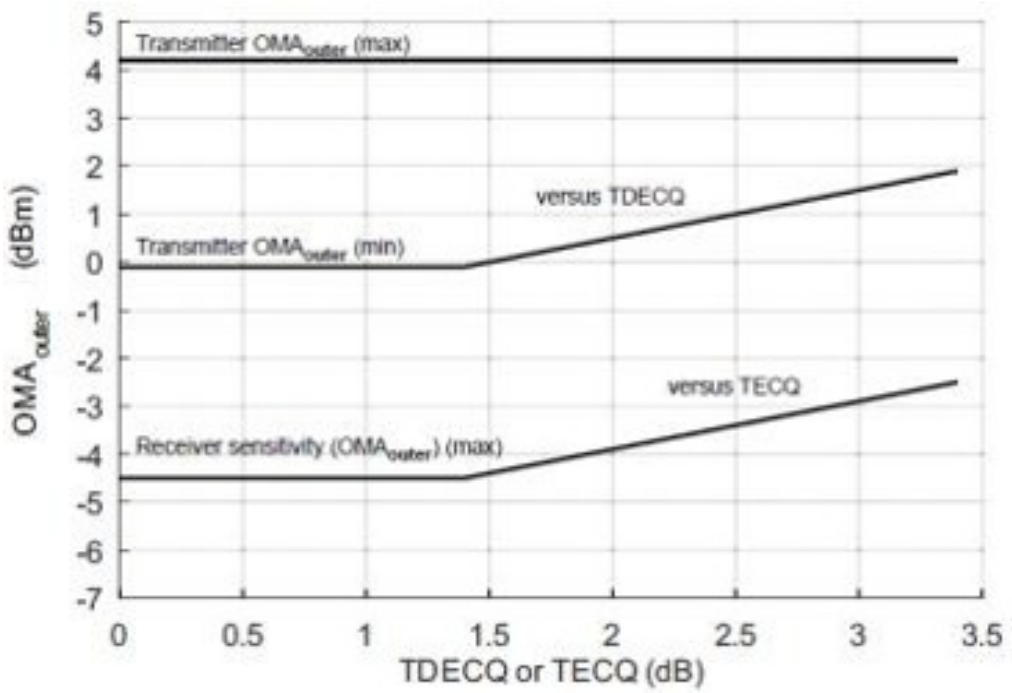
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1265.25	1271	1276.75	nm	
	L1	1285.25	1291	1296.75	nm	
	L2	1305.25	1311	1316.75	nm	
	L3	1325.25	1331	1336.75	nm	
	L4	1265.25	1271	1276.75	nm	
	L5	1285.25	1291	1296.75	nm	
	L6	1305.25	1311	1316.75	nm	
	L7	1325.25	1331	1336.75	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Total average launch power				9.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-3.2		3.5	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	Max(−0.2, −1.6+TDECQ)		3.7	dBm	2
Difference in launch power between any two lanes (OMA_{outer})				4	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each Lane	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/under-shoot				22	%	
Transmitter peak-to-peak power				4.5	dBm	
Extinction Ratio	ER	3.5			dB	
$RIN_{17.1}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-16	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				

Optical Characteristics (Continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Damage Threshold, each Lane	TH_d	4.5			dBm	3
Average Receive Power, each Lane		-7.2		3.5	dBm	4
Receive Power (OMA_{outer}), each Lane				3.7	dBm	
Difference in receive power between any two lanes (OMA_{outer})				4.1	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation (1)	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-2.6	dBm	6
Bit Error Ratio Floor	BER_FL			3.4×10^{-6}		7
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-16	-13	-10	dBm	
LOS De-assert	LOSD	-15	-11	-7	dBm	
LOS Hysteresis	LOSH	1	2	3	dB	
Conditions of Stress Receiver Sensitivity Test (Note 8)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
OMA_{outer} of each aggressor lane			1.5		dBm	

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for OMA_{outer}(min) vary with TDECQ. Figure 5 illustrates this along with the values for OMA_{outer}(max).
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5: RS = max(−4.6, TECQ − 6.0) dBm (1), where RS is the receiver sensitivity and TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.
6. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.
7. Measured with a reference transmitter to produce SECQ greater than or equal to 2 dB. The BER at the receiver must stay within the specified limit over an OMA range of (−4.9+TDECQ) dBm to 3.7 dBm.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel bias current monitor absolute error	DMI_Ibias_Ch	-10	10	%	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

1. Due to measurement accuracy of different single mode fibers, there could be an additional ±1 dB fluctuation, or a ±3 dB total accuracy.

Mechanical Drawing

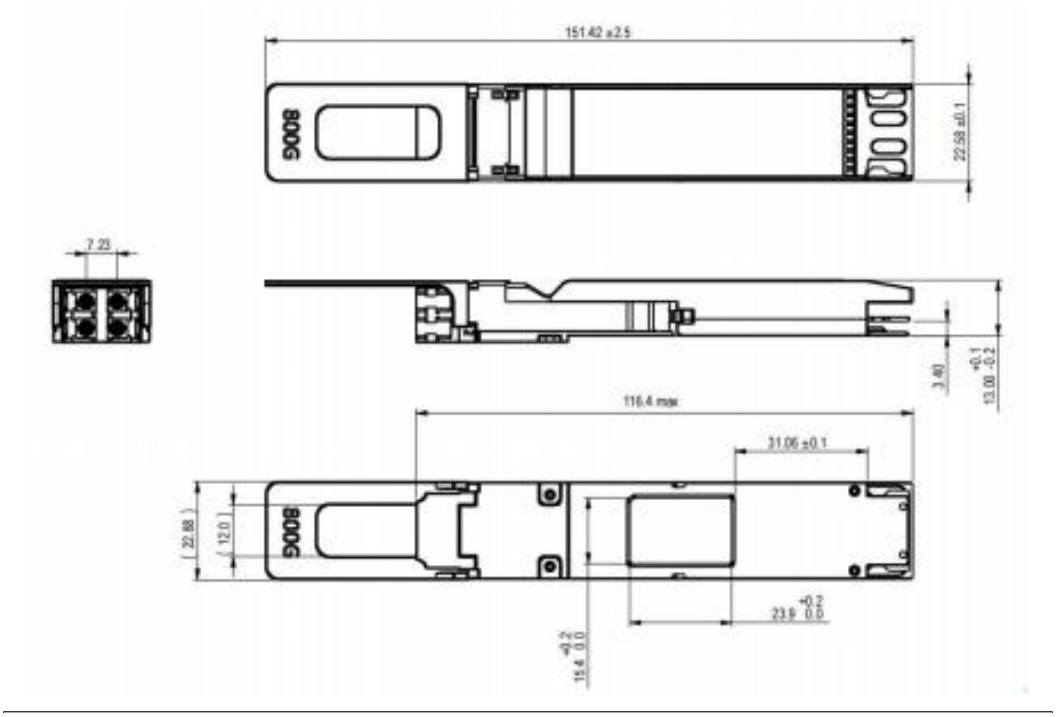


Figure 6. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.