FluxLight
OPTICAL TRANSCEIVERS

Datasheet

MMS1V90-WR-FL

400G, QSFP-DD, Duplex LC, CWDM 1271–1331nm, SMF, 10km, COM

Quick Spec

Rate Category:	400G
Form Factor:	QSFP-DD
Interface Type:	400G-LR4-10
Standard / Protocol:	100G Lambda MSA 400G-LR4-10; IEEE 802.3bs 400GAUI-8; QSFP-DD MSA
TX Wavelength:	1271/1291/1311/1331nm (CWDM)
RX Wavelength:	1271/1291/1311/1331nm (CWDM)
Cable Type:	SMF
Reach:	10km (SMF) with host FEC
DDM:	Supported
Connector Type:	Duplex LC
Power Consumption:	12W max
Operating Temperature:	0°C to +70°C (COM)



Overview

The FluxLight MMS1V90-WR-FL is a 400Gb/s QSFP-DD optical transceiver for 400G links up to 10 km over duplex single-mode fiber. It converts eight 53.125 Gb/s PAM4 electrical lanes (400GAUI-8) into four 100G PAM4 optical lanes on the CWDM grid at 1271, 1291, 1311 and 1331 nm, multiplexes them onto one fiber, and reverses the process on the receive side. A DSP gearbox with integrated retimers handles the 8-to-4 lane conversion.

The module complies with the 100G Lambda MSA 400G-LR4-10 specification and the QSFP-DD MSA (Type 2), uses a duplex LC connector, draws 12 W maximum from a single +3.3V supply, and provides real-time digital diagnostic monitoring. Host FEC is required to support the full 10 km reach.

Features

- QSFP-DD MSA compliant (Type 2), hot-pluggable
- 100G Lambda MSA 400G-LR4-10 specification compliant
- 8 × 53.125 Gb/s PAM4 electrical interface (400GAUI-8)
- 4 CWDM lanes at 1271/1291/1311/1331 nm, 106.25 Gb/s PAM4 per lane, with MUX/DEMUX
- Up to 10 km over single-mode fiber with host FEC
- Duplex LC connector
- Average launch power −2.8 to +4.0 dBm per lane; stressed receiver sensitivity −4.1 dBm (OMAouter)
- Digital diagnostic monitoring
- Single +3.3V power supply, 12 W maximum power consumption
- Operating case temperature: 0°C to +70°C (COM)
- RoHS compliant, Class 1 laser product
- 100% compatible with and programmed for the target OEM platform
- Backed by a FluxLight lifetime warranty

Applications

- 400G Ethernet over duplex single-mode fiber up to 10 km
- Data center interconnect and campus links
- Enterprise networking

Functional Description

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver and EML lasers together with an optical multiplexer. On the receiver path, an optical de-multiplexer is coupled to a 4 channel photodiode array. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and also an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to the 100G Lambda MSA 400G-LR4-10 specification with duplex LC connector.

Transceiver Block Diagram

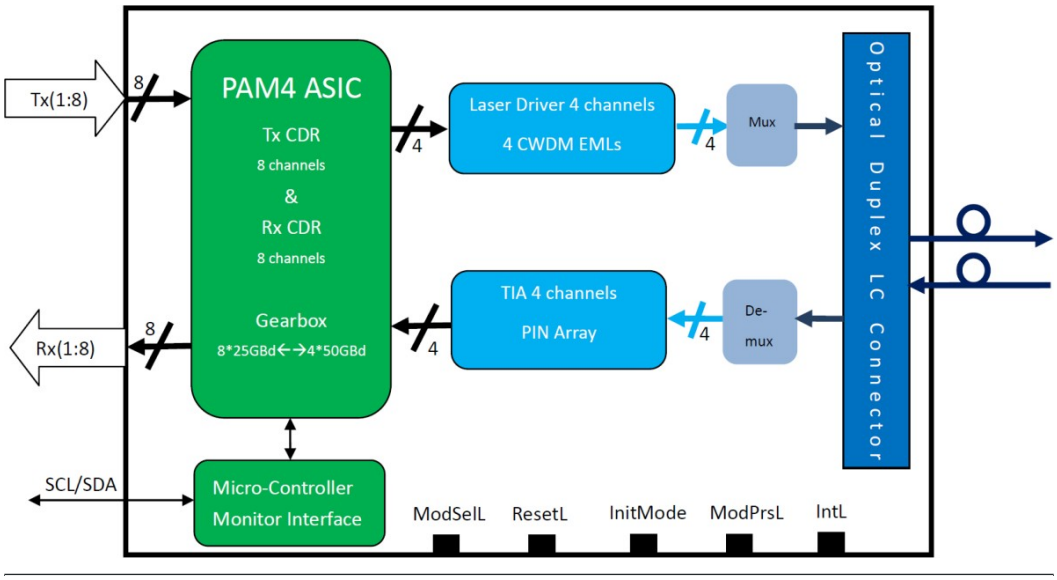
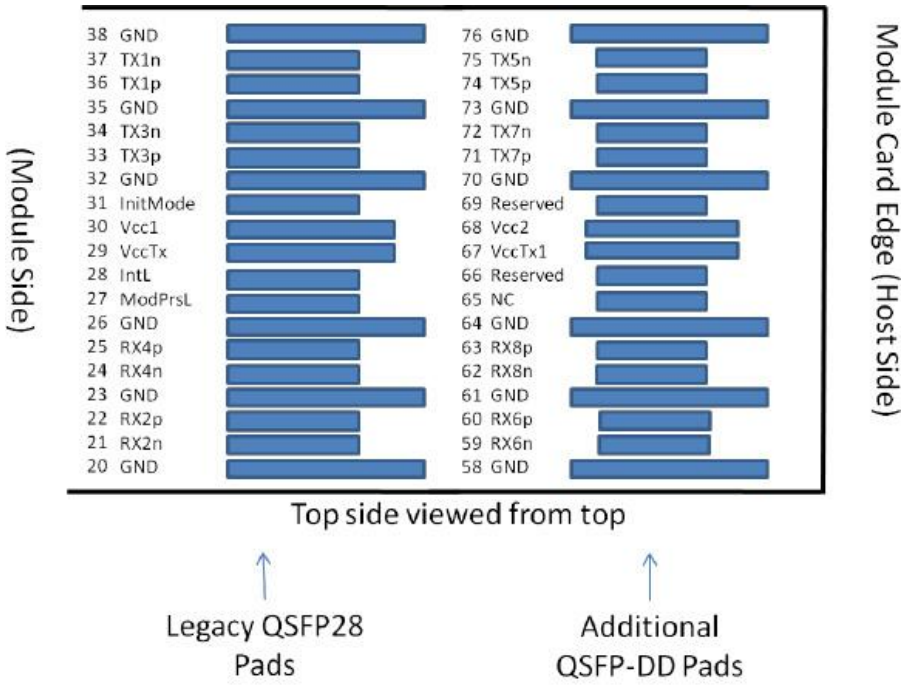
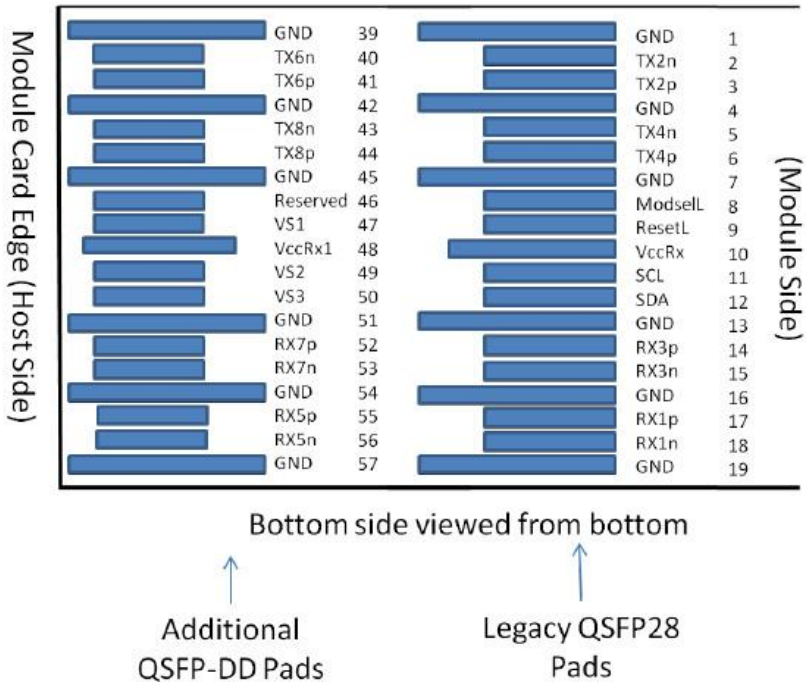


Figure 1. Transceiver Block Diagram

Pin Assignment and Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.


(Module Side)
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 InitMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 Reserved
68 Vcc2
67 VccTx1
66 Reserved
65 NC
64 GND
63 RX8p
62 RX8n
61 GND
60 RX6p
59 RX6n
58 GND
Module Card Edge (Host Side)
Top side viewed from top
Legacy QSFP28 Pads
Additional QSFP-DD Pads


Module Card Edge (Host Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModselL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19
(Module Side)
Bottom side viewed from bottom
Additional QSFP-DD Pads
Legacy QSFP28 Pads

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode (called LPMode in legacy QSFP applications)	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	

Pin Assignment and Description (Continued)

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2

Pin Assignment and Description (Continued)

Pin #	Logic	Symbol	Description	Plug Sequence	Notes
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kohms and less than 100 pF.

Recommended Power Supply Filter

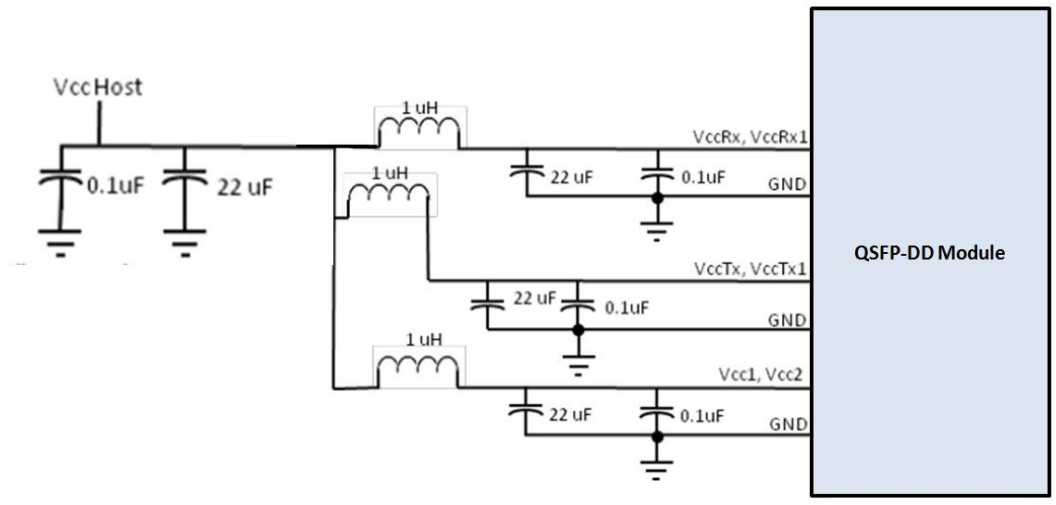


Figure 3. Recommended Power Supply Filter

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Power Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensation)	RH	0	85	%
Damage Threshold, each Lane	TH_d	5.0		dBm

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.002		10	km	2

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	

Electrical Characteristics (Continued)

Parameter	Test Point	Min	Typical	Max	Units	Notes
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)			dB	
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)			dB	
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	

Optical Characteristics (Continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			10.0	dBm	
Average Launch Power, each Lane	P_{AVG}	-2.8		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	0.2		4.2	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lane, for ER ≥ 4.5 dB		-1.2			dBm	
Launch Power in OMA_{outer} minus TDECQ, each Lane, for ER < 4.5 dB		-1.1			dBm	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.9	dB	
TDECQ – $10*\log_{10}(C_{eq})$, each Lane				3.9	dB	3
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	dB	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			15.6	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-20	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5.0			dBm	5
Average Receive Power, each Lane		-9.1		4.0	dBm	4
Receive Power (OMA_{outer}), each Lane				4.2	dBm	
Difference in Receiver Power between any Two Lanes (OMA_{outer})				4.6	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			max(−6.6, SECQ − 8.0)	dBm	6
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.1	dBm	7
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-20			dBm	
LOS De-assert	LOSD			-12.1	dBm	

Optical Characteristics (Continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stressed Receiver Sensitivity						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.9		dB	
SECQ – $10*\log_{10}(C_{eq})$, Lane under Test				3.9	dB	
OMA_{outer} of each Aggressor Lane			0.5		dBm	

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMAouter (min) must exceed the minimum value specified here.
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.9 dB. It should meet Equation (1), which is illustrated in Figure 4: RS = max(−6.6, SECQ − 8.0) dBm (1), where RS is the receiver sensitivity and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.
7. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

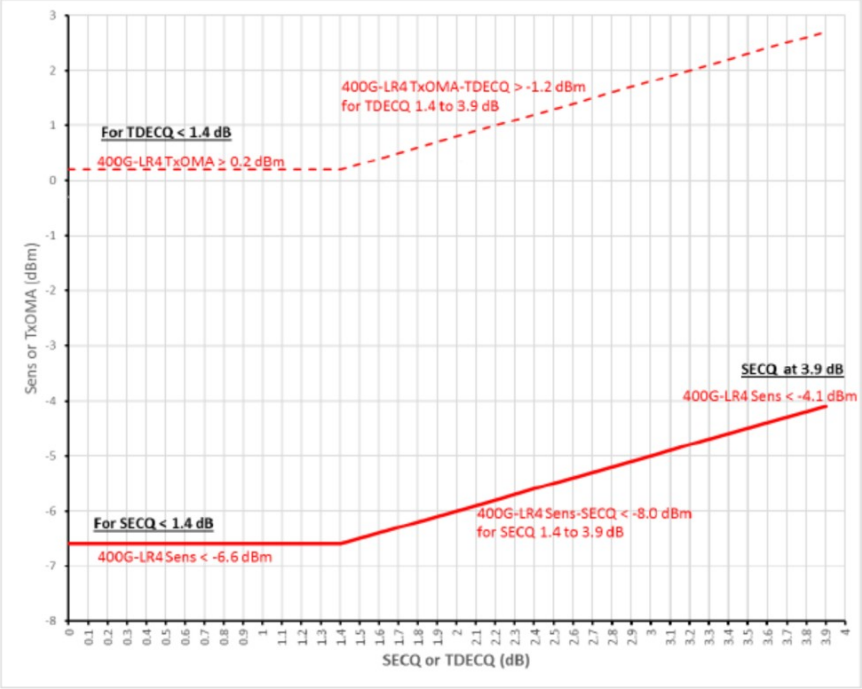


Figure 4. Illustration of Receiver Sensitivity Mask for 400G-

Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel bias current monitor absolute error	DMI_Ibias_Ch	-10	10	%	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Dimensions

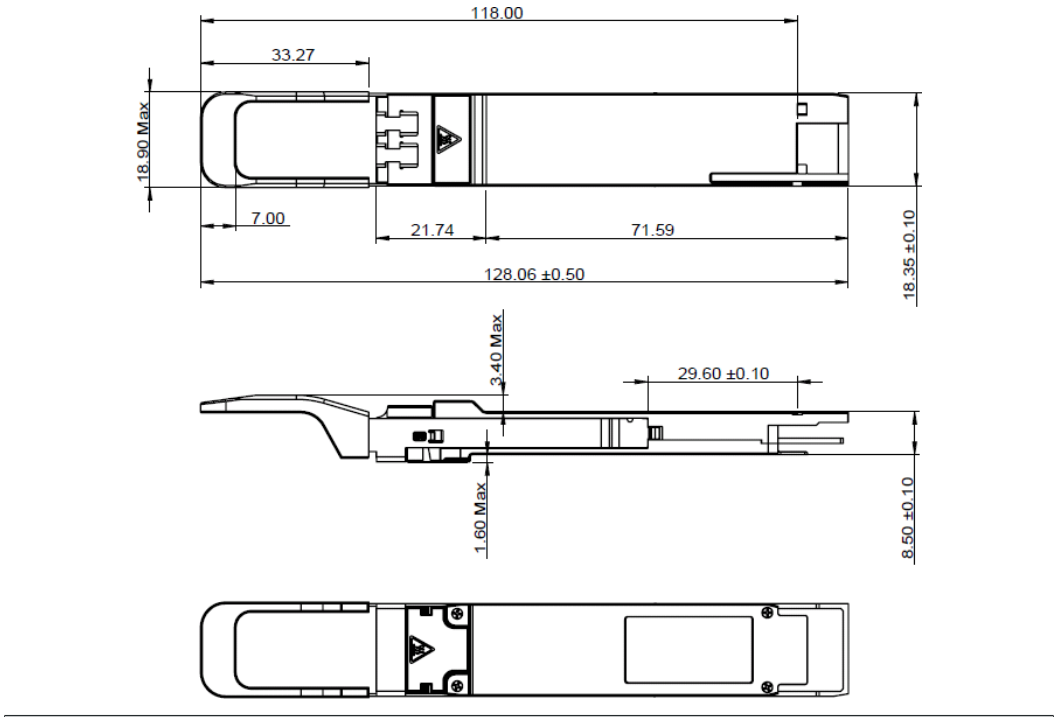


Figure 5. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.